ABSTRACT

A circuit, apparatus and method for maximizing system margins by adjusting a duty-cycle of a clock signal in a receive circuit to whatever duty-cycle is optimal for the particular incoming serial data, rather than the typical 50% duty-cycle, is provided in embodiments of the present invention. A receive circuit, including duty-cycle-correction logic, is included in a double-data rate communication apparatus having a transmit circuit transmitting serial data having duty-cycle distortion. A receive circuit includes a first and second sampler to obtain data and edge values of an incoming serial data responsive to a data and edge clock, respectively. A duty-cycle-correction logic generates a duty-cycle-correction signal to a duty-cycle clock integrator that adjusts the edge clock signals while maintaining quadrature to the data clocks. In an embodiment of the present invention, a duty-cycle-correction logic includes an evaluator circuit to generate an up or down signal responsive to the data and/or edge values. In a further embodiment of the present invention, an evaluator circuit is coupled to a counter and a DAC to generate a duty-cycle-correction signal to the duty-cycle clock integrator. A digital filter or coding scheme is also used to reduce the likelihood of misinterpreting malevolent incoming serial data for duty-cycle distortion in an embodiment of the present invention.